JOB NO.

CONQUEST

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CIRCUIT BOARD DESIGN GUIDELINES

Customer Information:

Company Name _____

Street Address _____

City, State and Zip _____

Board Name _____

Board No. _____Rev_____ Program Name _____

Assembly No. _____Rev_____ Purchase Order _____

Purchasing Contact:

Primary _____ Phone Number _____

Email Address _____ Fax Number _____

Technical Contacts:

Primary _____ Phone Number _____

Email Address _____ Fax Number _____

Other Contact _____ Phone Number _____

Email Address _____ Fax Number _____

Other Contact _____ Phone Number _____

Email Address _____ Fax Number _____

Other Contact _____ Phone Number _____

Email Address _____ Fax Number _____

Prepared By _____ Date _____

Note: All dimensions contained in this document are in inches. Dimensions enclosed by **"[ ]"** are Conquest defaults and will be used unless otherwise specified. In addition, all dimensions specified herein are artwork dimensions and do not compensate for unique manufacturing tolerances.

1. **Design Technologies Utilized (Please check all that apply):**

Digital	Lead-Though Board Parts	Controlled Impedance
Analog	Surface Mount Parts	Differential Pair
RF	One Side Both Sides	Backplane/Motherboard
High Voltage	Hybrid/Custom Parts	Paired (Mating) Boards
Buried Resistor	Heatsink or Thermal Plane	C.O.B. (Chip On Board)
PCI	Buried Capacitance	Multiple Chip Module (MCM)

2. **Customer Provided Reference Drawings:**

Schematic Drawing No. _____ Rev.____ No. Pages ____
Mechanical Drawing No. _____ Rev.____ No. Pages ____
Placement Drawing No. _____ Rev.____ No. Pages ____
Heatsink Drawing No. _____ Rev.____ No. Pages ____
SMD Footprint Dwg. No. _____ Rev.____ No. Pages ____
Other: _____ Rev.____ No. Pages ____

3. **Specifications / Standards (Please check all that apply):**

UL 94V.0	[IPC-2220 Series]	NHB 5300 (NASA)	ISO 9000
[IPC-A-600]	MIL-P-55110	MIL-P-50884	WS 6536
IPC-6011/6012	DOD-STD-2000	IPC-FC-250	IPC-ML-950

Customer Statement of Work No. _____ Dated_____
Customer PWB Design Specification No. _____ Rev._____
Customer Fabrication Specification No. _____ Rev._____
Customer Auto-Assembly Specification No. _____ Rev._____
Customer Heatsink Design Specification No. _____ Rev._____
Other: _____ Rev._____

4. **Primary Interconnect Information To Be Supplied To Conquest:**

Schematic drawings for manual netlist creation	Basic ASCII netlist file
Signal ordered netlist file (ECL or serial routing)	Cadence Allegro® *.brd* file
Placed netlist file (x,y coordinates for all pins)	Cadence Concept® *pst* files
Signal ordered placed netlist file (ECL routing)	Gerber files
DXF or AutoCAD® *.dwg* files	Other: _____

Name of CAD/CAE system netlist was generated from: _____

5. **Components Placement (General):**

A. Defined as:

Fixed - Conquest will not relocate components without explicit permission from the customer.

Partially fixed - Conquest to determine placement of all components except those specified by the customer as being fixed.

Semi-fixed - Conquest will maintain the relative component placement as specified by the customer but may slightly alter the exact component locations to enhance routability.

Suggested - Conquest may alter the placement as necessary for routability.

Unspecified - Conquest is to determine the parts placement.

B. Connector pin assignments are: O [Fixed] O Permutable

C. Is IC Gate swapping permitted? O Yes O [No]
If yes, within IC only from one IC to another

D. Bypass (Decoupling) Capacitors are required for every ___ IC's,
or defined per fixed/suggested placement.

E. Are spare IC pad patterns required? O Yes O [No]
If yes, please specify quantity, types and what power/ground connections are required, in the comments section on page 5.

F. Are all components required to be located on a specific grid increment with respect to a datum tooling hole? O [Yes] O No

If yes, increment is to be: .050" .025" [.005"] Other:_____

G. Is a specific component orientation required? O Yes O [No]
If yes, guidelines must be supplied.

H. Are auto-assembly design rules required? O Yes O [No]
If yes, specifications or guidelines must be supplied.

I. Are components to be renumbered after Placement ? O Yes O [No]

If yes, before placement review, [after placement approval], or after routing?
If yes, spares are included or skipped in renumbering.
If yes, what renumbering convention is to be used if other than left to right, top to bottom? (Describe in comments section on Page 5)

J. Component Clearance Requirements:
Minimum part to part body spacing (air gap): _____ [.010"]
Minimum part body to board edge (air gap): _____ [.050"]
Minimum part body to tooling hole (air gap): _____ [.050"]

6. **Through-Board-Mount Leaded Components**

A. Plated through holes and pads All PTH & pad sizes supplied

1. PTH diameter to be _____[.010"] greater than maximum lead diameter

2. Square pads required to indicate pin #1? O [Yes] O No
   If yes, all parts [IC's, polarized parts and connectors]
   If yes, all layers [on external layers only]

3. Graphic symbols required to indicate polarity? O [Yes] O No
   If yes, in etch on layer #_____, or [on silkscreen]

   Note: If specific graphic symbols are required, please describe in the component placement comments section or provide specific guidelines.

7. **Surface Mount Components**

A. SMD footprint patterns are: O supplied O [IPC-SM-782] O other criteria supplied

1. Vias associated to SMD land patterns are:
   - permitted to be embedded in the land area O Yes O [No]
   - permitted to be located under the IC O [Yes] O No
   - to be accessible after component placement O [Yes] O No
     from component side [from solder side] from either side

   Minimum width of trace (stringer) connecting the land to its associated via:
   signal:_____[.008"] power/ground:_ _____[.010"]

   Minimum length of trace (stringer) from edge of land to edge of its associated via-pad:_____[.008"]

   Minimum clearance from land to other via-pads of footprint pattern (air gap):_____[.008"]

   Are associated vias required for SMD lands which will have no connections (i.e. unused pins)? O Yes O [No]

   Routing directly to the SMD land is: [permitted] required not permitted

2. Finished PTH diameter of vias associated to SMD lands: _____[.015"]

3. Plated through hole tolerance: +/- _____[.003"]

4. External layer associated via pad diameter: _____[.045"]

5. Internal layer associated via pad diameter: _____[.038"]

8. **Component Placement Comments**

Define below any critical placement requirements or what reference is to be used for any critical placement requirements (i.e. drivers, test points, LED's, terminators, etc.)

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

_____

9. **Routing (Wiring)**

A. Minimum signal routing trace width, internal layers:_____[.008"]

Note: If multiple trace widths are to be used, define in the comments section on page 9.

B. Minimum signal routing trace width, external layers:_____[.008"]
or no wiring allowed on external layers

C. Minimum trace width for power/ground wiring:_____[.025], or N/A

Note: If power/ground to be connected other than planes, define net names and required trace widths in the routing comments section on page 9.

D. Minimum trace to trace clearance required (air gap): _____[.008"]

E. Minimum trace to pad clearance required (air gap): _____[.008"]

F. Inner layer artwork to contain: [all pads] used pads only

G. Minimum copper to Tooling PTH's clearance (air gap)

Internal layers: _____[.030"]

External layers: _____[.030"]

(Routing Continued)

H. Minimum copper to board edge clearance (air gap)

Internal layers: _____[.050"]

External layers: _____[.050"]

I. Routing vias permitted under components: O [Yes] O No

If yes, please note any exceptions (i.e. metal case components) in the comments sections on page 9.

J. ECL/serial routing required? O Yes O No

If yes, stringing order is: defined in netlist
to be determined by Conquest
other guidelines supplied

10. **Power/Ground Planes** **O Not Required**

A. Type of Power/Ground planes to be used:
solid plane layer
partial plane (entire layer not used for power/ground)
crosshatched (gridded conductors) plane

B. Width of PTH clearance annular ring:_____[.010"]

C. Are thermal relief patterns required for lead-thru-board connections? O [Yes] O No
If yes, minimum number of ties (straps) per PTH connection:_____[2]
If yes, minimum trace width of ties (straps):_____[.010"]

D. Are thermal relief patterns required for via connections? O [Yes] O No
If yes, minimum number of ties (straps) per PTH connection:_____[2]
If yes, minimum trace width of ties (straps):_____[.010"]

E. Split planes are: required [permitted] not permitted
If permitted or required, void width between planes:_____[.030"]
(Note: If required, define in comment section on page 9.)

F. Signal traces permitted on power/ground planes? O Yes O [No]

11. **Routing/Wiring Vias (Feedthroughs)**

A. Buried vias are: O permitted O [not permitted] O required

B. Blind vias are: O permitted O [not permitted] O required

C. Finished plated through hole (PTH) diameter:_____[.015"]

D. Plated through hole tolerance: +/- _____[.003"]

(Routing Vias Continued)

E. External layer pad diameter: _____[.045"]

Pad type: O [round] O square O other _____

F. Internal layer pad diameter: _____[.038"]

Pad type: O [round] O square O other _____

G. Aspect ratio check: $\frac{\text{maximum PWB thickness}}{\text{minimum PTH diameter}}$ = $\frac{\text{in.}}{\text{in.}}$ = _____

12. **Bonded Heatsink/Thermal Plane Requirements** **O Not Required**

A. Type of design:
External bonded heatsink, fixed design
External bonded heatsink, Conquest to design
External thermal plane
Internal thermal plane

B. Material: O Copper O Aluminum O Other: _____

Thickness:_____ Hardness:_____

C. Method of attachment to PWB:
Laminate
Spray adhesive
Hardware
Other: _____

D. Minimum clearance from component pad (air gap): _____[.030"]

E. Minimum clearance from non-plated holes (air-gap): _____[.030"]

F. Any electrical connection required (i.e. ground)? O Yes O [No]

If yes, to what signal name? _____

G. Heatsink related documentation to be supplied by Conquest:

[Fabrication drawing]
Drill template artwork
Geometry artwork
None required

13. **Layer Count**

A. Preferred total no. of layers: _____ (including planes and pads only layers)

B. Estimated no. of wiring layers: _____

C. Estimated no. of plane layers: _____

D. Estimated no. of cap layers: _____ (pads only external layers)

E. Estimated no. of other layers: _____ Type: _____

14. **Design Layer Descriptions**

Layer	Layer Name	Special Design Requirement Notes
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32		
33		
34		
35		
36		

15. Routing Comments:

_____

_____

_____

_____

_____

_____

_____

16. **Silkscreen Design** **O Not Required**

A. Silkscreen is required: O top side O bottom side O both sides

1. [All component designations]: O top side O bottom side
2. Only IC component designations: O top side O bottom side
3. [All component outlines]: O top side O bottom side
4. Only IC component outlines: O top side O bottom side
5. Alphanumeric grid (matrix) type: O top side O bottom side

B. Color:_____[white]

C. Minimum text height to be:_____in.

Note: Unless otherwise specified text size may vary and minimum text height will be .050 inches.

17. **Solder Mask Designs** **O Not Required**

A. Solder mask is required: O top side O bottom side O both sides

B. Minimum annular ring for PTH pads and SMD lands: _____in. [.005"]

C. Minimum annular ring for nonplated through holes: _____in. [.005"]

D. Minimum clearance (air gap) to board edge: _____in. .050" or [Flush]

E. SMD land-associated vias to be tented (covered)? O Yes O [No]

F. Routing vias to be tented (covered)? O Yes O [No]

G. Solder mask over bare copper (S.M.O.B.C.)? O [Yes] O No

H. Type: SR 1000 [LPI mask] Dry film Other:_____

18. **Solder Paste Mask (Stencil) Design** **O Not Required**

A. Solder paste is required: O top side O bottom side O both sides

B. Solder paste mask footprint patterns to be:

[same size as SMD land patterns]

_____in. annular ring smaller than SMD land patterns

_____in. annular ring greater than SMD land patterns

19. **Conformance Test Coupons** **O None Required**

Type: MIL-P-55110 IPC-6011/6012

Controlled impedance coupon, Conquest to determine type
Controlled impedance coupon with specification to be supplied
Flexible circuit test coupon
Nonstandard coupon with unique specifications to be supplied

20. **Fabrication (General)**

A. Board thickness requirement:_____in. +/- _____in.

To be measured over: O laminate O circuitry O solder mask

Note: Minimum board thickness using 1 ounce copper will be .0062" multiplied by the total number of layers.

B. Type of material (i.e. FR-4, Polyimide, etc.):_____

C. Controlled impedance is: O required O not required

If required, parameters to be determined by Conquest? O Yes O No
If no, impedance parameters must be supplied.

D. Bare board electrical test is: O required O not required

Comparison board electrical test ("golden board"), or
[IPC-D-356 CAD netlist electrical test]

E. S.M.O.B.C. required: O No O solder level (.0001 min.) O solder plate (.0003 min.)

F. Gold plate required: O No O Yes, No. of board edges:_____

Type: Immersion Electroplated

Thickness: _____[50m] Gold over _____[100m] Nickel

G. Hole fill required: O No O Yes, fill with:_____

H. Panelization required? O No Type: Routed V-Scoured

Panel size:_____in. x _____in. No. up:_____

or to be determined by Conquest

Rail required: 2 sides 4 sides Minimum rail width: _____ [.250]

21. **Fabrication Layer Stack-up**

Layer Number	Nominal Thickness	(Cu Wt.)	Nominal Impedance
1 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
2 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
3 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
4 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
5 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
6 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
7 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
8 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
9 →	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____Dielectric/B-stage		
10→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
11→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
12→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
13→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
14→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
15→	---------- ← _____ Copper	_____oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
16→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
17→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
18→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
19→	---------- ← _____ Copper	_____oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
20→	---------- ← _____ Copper	_____oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
21→	---------- ← _____Copper	_____oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		

(**Fabrication Layer Stack-up continued)**

Layer Number	Nominal Thickness	(Cu Wt.)	Nominal Impedance
22→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
23→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
24→	---------- ← _____ Copper	_____oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
25→	---------- ← _____ Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
26→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
27→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
28→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
29→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
30→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
31→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
32→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
33→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
34→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
35→	---------- ← _____Copper	_____ oz.	_____ohms
	[=====]← _____ Dielectric/B-stage		
36→	---------- ← _____Copper	_____ oz.	_____ohms

Dielectric thickness tolerance: +/-_____in. or _____ %

Controlled impedance tolerance: +/-_____[10] ohms or _____ %

22. **Miscellaneous Comments**

_____

_____

_____

_____

_____

23. **Deliverable Items (Please check all that apply)**

A. Design Review Cycles

Individual footprint patterns:	O 1:1	O 2:1	O Other _____
Components placement:	O 1:1	O 2:1	O Other _____
Critical routing:	O 1:1	O 2:1	O Other _____
Final design:	O 1:1	O 2:1	O Other _____
Other: _____	O 1:1	O 2:1	O Other _____
Other: _____	O 1:1	O 2:1	O Other _____

Media for review: O Paper checkplots O Allegro *.brd* file
O Gerber files O DXF files
O HPG plot files O AutoCAD DWG files
O Other: _____

B. Photoplotted Artwork (.007 film) O Yes O Not Required

Number of sets required:_____

(To include all board layers, silkscreens, solder masks and solder paste masks)

C. NC Drill Files O [Yes] O Not Required

D. IPC-D-356 Netlist File O [Yes] O Not Required

E. ATE Electrical Test Files O Yes O Not Required

[One test point per net], or One test point per node

To be accessible from: component side [solder side] either side

F. Gerber Plot Files O [Yes] O Not Required

Is there a limitation to no. of apertures used? O Yes O [No]
Is there a specific aperture table to be used? O Yes O [No]
If yes, aperture definitions must be supplied.

G. Reference Designator Back Annotation O [Yes] O Not Required

Cadence Concept® back annotation files
Was/Is listing text file
Manual Back Annotation (to "mark-up" customer's schematics)

H. Documentation Drawings O [Yes] O Not Required

Drawing Standard: Commercial MIL-STD Level 1 MIL-STD Level 3

[PCB Fabrication (drill/trim) Drawing], No. of sheets:_____ sheet size:_____

Artwork Continuation sheets, No. of sheets:_____ sheet size:_____

(H. Documentation Drawings Continued)

[PCB Assembly Drawing], No. of sheets:_____ sheet size:_____

Heatsink Fabrication Drawing, No. of sheets:_____ sheet size:_____

Other _____, No. of sheets:_____ sheet size:_____

Other _____, No. of sheets:_____ sheet size:_____

Type of media: O Paper checkplots O Allegro *.brd* file
O Gerber files O DXF files
O HPG plot files O AutoCAD DWG files
O Other: _____

Note: Customer to supply sample drawing formats, applicable notes, details, etc.

I. Manhattan vs. Routed Signal Length Report O Yes O Not Required

J. Parallelism Report O Yes O Not Required

K. ECL/Serial Route Report O Yes O Not Required

Corresponding to: Original schematic reference designations
Renamed assembly reference designations

L. Other (Define)

_____

_____

_____

_____

_____

_____

M. Other (Define)

_____

_____

_____

_____

_____

_____

_____

~ End of Guidelines Document ~