1. Course Introduction

- course deals with the fabrication of electronic packaging substrates
- electronic package = structure used to interconnect, power, cool, and protect integrated circuits (ICs) for electronic systems and products

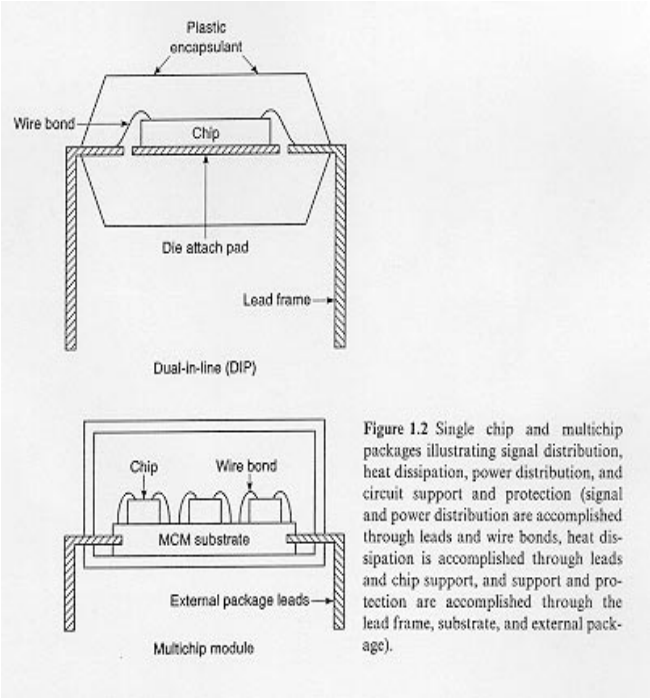


Figure 1.2 Single chip and multichip packages illustrating signal distribution, heat dissipation, power distribution, and circuit support and protection (signal and power distribution are accomplished through leads and wire bonds, heat dissipation is accomplished through leads and chip support, and support and protection are accomplished through the lead frame, substrate, and external package).

Analogy: *IC* = brain, *Package* = body

- electronics is a $300B world market, and packaging is a significant portion of that total which affects the following industries:

  - computing
  - telecommunications
  - aerospace
  - automotive
  - consumer electronics

- up until a few years ago, the performance of an IC was impacted little by the package;

  BUT NOW: the point has been reached where advancements in IC performance are limited by packaging technology!!!

- To optimize IC performance, the package must provide:

  - improved electrical performance (i.e., less delay, low noise)
  - increase packaging density => miniaturization
  - low power consumption
  - high reliability

- fabricating a multichip module (MCM) electronic packaging substrate requires a sophisticated

sequence of dozens or hundreds of process steps, including:

- interconnect design
- polymer deposition
- photolithography
- metallization
- substrate testing

- in this course, we will go through a simple process sequence to make a 2-metal layer organic MCM substrate

2. Course Policies and Procedures (see handout)

3. Course Outline (see handout)

4. Packaging Hierarchy

- electronic systems consist of several layers of packaging, each with distinctive types of inter-connection devices:

Level 0: gate-to-gate interconnections on the chip
Level 1: chip-to-module connections
Level 2: board level interconnections
Level 3: board-to-board interconnections
Level 4: connections between sub-assemblies
Level 5: connections between systems (i.e., computer to printer)

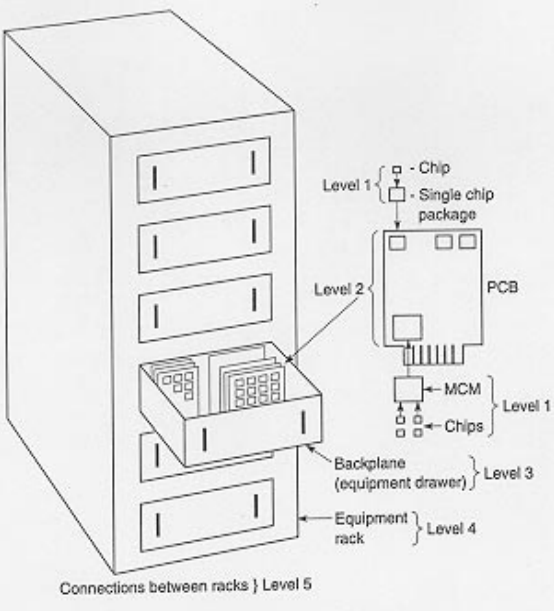
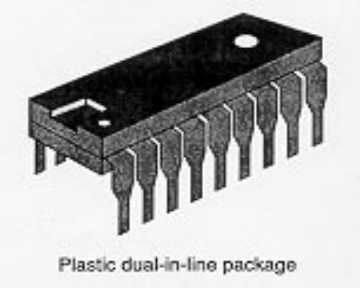


Figure 1.3 Electronic packaging hierarchy.

- this course concentrates on *Level 2*; the follow-on "Module Assembly" course focuses on *Level 1*

5. Evolution of Packaging Technology

- DIP = “dual-inline-package”; what most people envision when they think of an IC “chip”
  - ❍ developed in the 1960’s
  - ❍ leads are perpendicular to the body of the package
  - ❍ ideally suited for insertion mounting onto printed wiring boards (PWBs) using plated through holes (PTH)



- surface mount technology (SMT)
  - ❍ developed in the 1970’s
  - ❍ leads don’t penetrate the PWB surface; ICs can be mounted on both sides => higher density
  - ❍ mounting accomplished by reflow solder technology
  - ❍ use small outline packages (SOPs), which are miniature DIPs

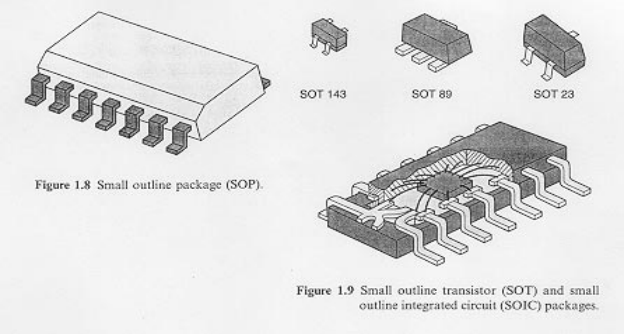
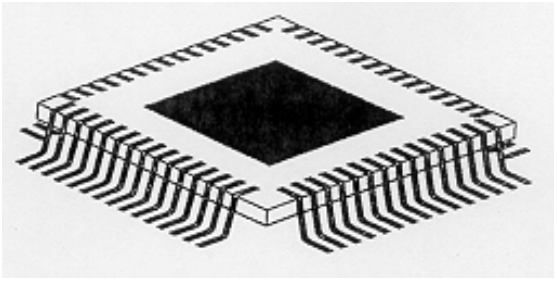
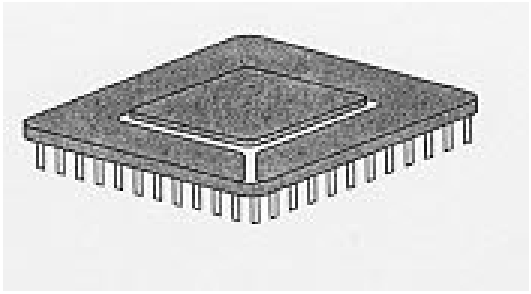


Figure 1.8 Small outline package (SOP).

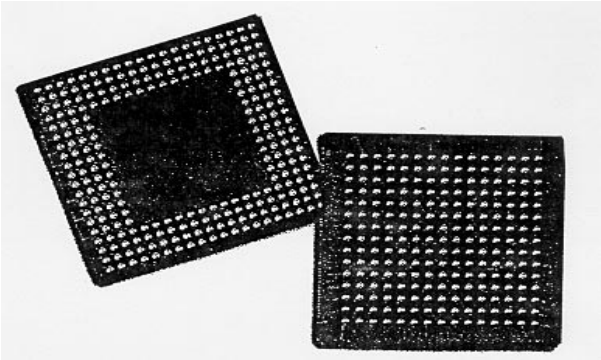
Figure 1.9 Small outline transistor (SOT) and small outline integrated circuit (SOIC) packages.

- quad flatpacks (QFPs) and pin grid arrays (PGAs)
  - ❍ developed in the 1980’s
  - ❍ leadless or leaded versions; plastic or ceramic bodies
  - ❍ have leads on all 4 sides => up to ~200 I/O’s
  - ❍ PGAs can have up to ~600 I/O’s

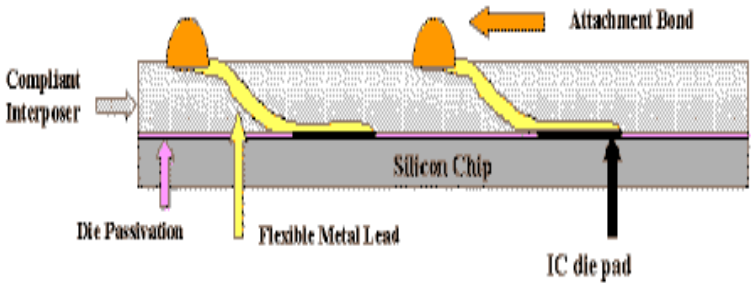




- ball grid arrays (BGAs)
  - ❍ developed in the early 1990's
  - ❍ replacement for QFPs
  - ❍ solder bumps in a matrix on the bottom of the package
  - ❍ higher density, smaller footprint, shorter electrical paths (i.e., *faster* signal propagation)
  - ❍ more expensive than QFP
  - ❍ natural choice for multichip module (MCM) packaging



- chip scale packages (CSPs)
  - ❍ developed in the late 1990's
  - ❍ extension of the bare IC to permit easy handling, testing, and assembly
  - ❍ about 1.2 times the size of bare die
  - ❍ offer a method for subjecting ICs to full functional and reliability testing while maintaining the approximate size and performance of a bare die
  - ❍ includes micro-ball grid array (μBGA), mini-BGA, and μSMT packages



- Major Motivation: pack more electronic functionality and higher speed performance into smaller volume

6. Driving Forces for Packaging Technology

- Major Issues: manufacturing cost, size and weight, signal integrity, heat dissipation, mechanical stability, testability, reliability

- *Manufacturability and Cost*:

  ❍ includes materials, fabrication steps, and the cost of the IC
  ❍ costs also incurred from testing, rework, yield loss
  ❍ manufacturability depends on process control, cycle time, repairability, equipment downtime, design tolerances

- *Electrical Design*:

  ❍ interconnect speed now plays a dominant role in determining performance limits
  ❍ each connection has parasitic capacitance, resistance, and inductance that limit speed, potentially distort signals, and add noise
  ❍ leads for connections are also a source of reliability problems
  ❍ several factors need to be considered, including:
    - lead length
    - matched impedances
    - low ground resistance
    - simultaneous switching and power supply spiking

- *Thermal Design*:

  ❍ objective = remove heat from the junctions of the ICs (to keep dopants from moving)
  ❍ techniques = forced air, liquid cooling
  ❍ considerations:
    1) how to remove heat (from the front or backside of the IC)
    2) air or liquid?
    3) thermal conductivity of the substrate
    4) stresses induced due to CTE mismatches

- *Mechanical Design*:

  ❍ susceptibility to thermal stresses must be considered in design
  ❍ tensile modulus (“stiffness”) also a consideration

- *Testability*:

  ❍ 2 types:
    1) in-process testing (non-destructive)
    2) stress/reliability testing (destructive)
  ❍ for MCMs, 2 phases:
    1) substrate (this course)
    2) assembled module (next course)

7. MCM Definitions and Classifications

- multichip module (MCM) = single electronic package with multiple ICs
- advantages: miniaturization, electrical and thermal performance, reliability
- Categories:

  1) *laminated* (MCM-L) - constructed of plastic laminate-based dielectrics and copper conductors using PWB technology; lowest cost MCMs

2) *ceramic* (MCM-C) - constructed on cofired ceramic or glass-ceramic substrates using thick film (screen printing) technologies

3) *deposited* (MCM-D)- formed by the deposition and patterning of thin films; highest performance MCMs

- comparison:

Characteristic	MCM-L	MCM-C	MCM-D
Maximum Wiring Density (cm/cm^2)	300	800	250 - 750
Minimum Line Width (μm)	60 - 100	75 - 100	8 - 25
Line Spacing (μm)	625 - 2250	125 - 450	25 - 75
Via Diameter (μm)	300 - 500	100	8 - 25
Cost ($/$cm^2$)	3 - 30	50 - 1000	800 - 8000

- to optimize cost and performance trade-offs, the high performance of MCM-D at the low cost of MCM-L is desirable
- in this hybrid technology, called MCM-L/D, substrate structures are formed as multiple layers of metal separated by dielectric material
- Georgia Tech Packaging Research Center (PRC) “single-level-integrated module” (SLIM) implementation of the MCM-L/D paradigm: